REMARKS

This application has been reviewed in light of the Office Action dated November 13, 2007. Claims 1-7 are now pending in the application. Claim 1 has been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the following remarks is respectfully requested.

By the Office Action, the Examiner requested the submission of the references cited in the application. A separate **Information Disclosure Statement** will be submitted.

Additionally, the Examiner has requested that a new title be submitted, asserting that the title of the invention is not descriptive. The Applicant respectfully disagrees with the Examiner's assertions. The claims are clearly directed to an active matrix liquid crystal display device. As such, it is respectfully submitted that a new title need not be submitted.

By the Office Action, claims 1-5 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,667,783 to Bae et al. (hereinafter 'Bae') in view of U.S. Patent No. 6,667,783 to Greene et al. (hereinafter 'Greene').

Claim 1 recites, inter alia, an "active matrix liquid crystal display device comprising ... sets of selection and data address conductors connected to the picture elements, and a set of connection lines for supplying selection signals to the set of selection address conductors, ... wherein each picture element includes a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements."

Bae and Greene, taken singly or in combination, fail to disclose or render obvious at least the claim features of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row. . . wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements." Bae is directed to forming a storage capacitor within a Liquid Crystal Display (LCD) without decreasing the aperture ratio of the display and without increasing the number of wires (see, e.g., Bae, column 2, lines 38-41). According to Bae, use of an independent storage electrode line (SL) within a row of pixels may decrease the aperture ratio of an LCD (see, e.g., Bae, column 2, lines 38-41) (see also FIG.1, illustrating the use of an independent storage electrode line). Additionally, Bae describes prior art methods of circumventing the use of an independent storage line as being problematic because, in such methods, a connection between a terminal of a storage capacitor and a gate line generates a parasitic capacitance in the gate line (see, e.g., Bae, FIG. 2; column 2, lines 22-25).

To avoid a decrease in aperture ratio and a parasitic capacitance, Bae proposes a liquid crystal display that has two or more storage capacitors (C_{ST}) connected to drain terminals of switches (Q) of two different pixels of the display (see, e.g. Bae, column 2, lines 44-47; column 2, lines 60-64) (see also, e.g., Bae, FIG. 3). This configuration forms a line of storage capacitors along a row of pixels (see, e.g., Bae, FIG. 3). Bae recognizes that the configuration results in floating terminals of storage capacitors at the ends of the rows (see, e.g., Bae, column 11, lines 37-40) and, to address the problem, Bae teaches a connection of the floating storage capacitor to a previous gate line (see, e.g., Bae, column 11, lines 56-64) (FIGS. 23, 24).

However, Bae does not disclose "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row. . .

wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements." Although Bae discloses a pixel configuration in which there is a connection between a floating storage capacitor and a gate line of a different row, the pixel configuration does not include a storage capacitor connected between a picture element electrode and a storage capacitor line. In the pixel configuration described in Bae, the pixel electrode (C_{LC} terminal) (82) is directly connected to the line of storage capacitors (see, e.g., FIG. 23; column 8, lines 4-11 (describing the pixel electrode's relationship with the line of storage capacitors)). A storage capacitor is not situated between a picture element electrode and a storage capacitor line, as recited in claim 1.

Indeed, the configuration of storage capacitors described in Bae cannot provide several beneficial LCD features that may, in contrast, be provided by aspects of the present principles. For example, according to aspects of the present principles, a storage capacitor line may be adapted to transmit both row address gating signals across a row of pixels and storage capacitor drive signals supplying a drive voltage across a row of pixels (see, e.g., Specification, p. 11, lines 17-26; p. 6, line 26 to p. 7, line 6) (see, also, FIG. 3, illustrating one configuration of a capacitor line 40 in accordance with one aspect of the present principles). This type of capacitive coupled drive scheme may improve the quality of the display by, for example, reducing image striking effects (see, e.g., Specification, p. 7, lines 2-6). Such signals cannot be transmitted through the line of capacitors disclosed in Bae, as the line itself is intermittently disjointed by storage capacitors (see, e.g., FIG. 24) (see also FIG. 9 & column 8, lines 7-11).

Furthermore, it should be noted that modifying the configuration described by Bae to include a storage capacitor connected between the picture element electrode and a capacitor line is not obvious to one of ordinary skill in the art, as such a modification would subvert the entire

principle of operation of Bae. As discussed above, Bae teaches the formation of a disjointed line of storage capacitors with terminals connected to different pixels to avoid a degradation of the aperture ratio of the display and a parasitic capacitance. Bae specifically teaches away from employing a storage capacitor between a pixel element electrode and a storage capacitor electrode line, as illustrated in FIG. 1 of Bae, because it states that use of the storage capacitor electrode line may decrease the display device's aperture ratio (see, e.g., Bae, column 2, lines 9-12).

Accordingly, Bae fails to disclose, suggest or render obvious the claim 1 feature of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row... wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements."

In addition, Greene also fails to disclose or render these features of claim 1 obvious. Nowhere does Green disclose or remotely suggest use of capacitor lines shared by picture elements in the same row. Accordingly, Bae and Greene, taken singly or in any combination, fail to render claim 1 obvious.

Thus, claim 1 is believed to be patentable over Bae and Greene. Moreover, claims 2-5 and 7 are believed to patentable over the cited references due at least to their dependencies from claim 1. As such, withdrawal of the rejection and allowance of the claims is respectfully requested.

Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Bae in view of Greene in further view of U.S. Patent No. 5,995,177 to Fujikawa et al. (hereinafter 'Fujikawa').

Claim 6 depends from claim 1 and includes all features recited in claim 1. Thus, claim 6 includes, inter alia, an "active matrix liquid crystal display device comprising ... sets of selection and data address conductors connected to the picture elements, and a set of connection lines for supplying selection signals to the set of selection address conductors, ... wherein each picture element includes a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements."

As discussed above, Bae and Greene fail to disclose or render obvious the features of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row... wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements." Indeed, Greene nowhere even mentions use of a capacitor line shared by picture elements in the same row. Furthermore, the combination of Bae and/or Greene with Fujikawa also does not render these features of claim 6 obvious.

Fujikawa is directed to an active matrix substrate with multi-layer signal lines and/or electrodes. According to Fujikawa, the described materials overlaying the signal lines avoid contact deficiencies resulting from oxidation of metal surfaces (see, e.g. Fujikawa, column 7, lines 50-52; column 7, line 65 to column 8, line 6; column 3, line 64 to column 4, line 11). Although Fujikawa mentions an LCD matrix having a storage capacitor connected between a capacitor line shared by pixel elements within a row (see, e.g., Fujikawa, FIG. 3), its

combination with Bae by one of ordinary skill in the art would not result in "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row... wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements," as included in claim 6.

Firstly, the capacitor line configuration disclosed in Fujikawa is essentially the same as the configuration including an independent storage electrode line (SL) (Bae, FIG. 1) discussed in Bae. As stated above, use of such a configuration is specifically taught against by Bae because of its tendency to decrease a display device's aperture ratio. Secondly, even if the capacitor line configuration disclosed in Fujikawa was implemented, its combination with Bae by one of ordinary skill in the art would not result in the features of claim 6 recited above. As discussed above, the connection between a gate line of a previous row with the line of storage capacitors in the Bae LCD was made to address the problem of a "floating" storage capacitor at the ends of a line of capacitors in the proposed matrix configuration. If the capacitor line configuration disclosed in Fujikawa were implemented, the floating storage capacitor problem would be removed by virtue of the storage capacitor's connection between a pixel element electrode and the capacitor line. As such, by combining Bae and Fujikawa, one of ordinary skill in the art would not conceive of "a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row... wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements," as included in claim 6.

In contrast to Bae, according to one aspect of the present principles, the coupling between a selection address conductor and a capacitor line associated with a different row may

be made to avoid incongruent brightness levels resulting from parasitic capacitance associated with connection lines (see generally, Specification, p. 9, line 27 to p. 11, line 24). This exemplary feature is not disclosed or in any way even remotely suggested by any of the references.

Accordingly, claim 6 is believed to be patentable over Bae, Greene and Fujikawa, taken singly or in any combination for at least the reasons discussed above. Thus, withdrawal of the rejection is respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives Deposit Account No. 14-1270.

Respectfully submitted,

Dated: 2-6-08

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